**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently amended) An improved protocol for devices comprising:

a serial bus for communication between a pair of devices;

communication on said serial bus between said devices utilizing a protocol comprising a plurality of digital bits in a predetermined format, said predetermined format comprising a frame;

said frame comprising a plurality of digital bits forming a framing cycle and a plurality of bits forming a data cycle, wherein the framing cycle provides a minimum bit transition frequency allowing clock recovery by the receiving device;

said devices formatting said digital bits in said predetermined frame format; said devices having no requirement for DC balance when formatting said digital bits, wherein said bits of said frame have an absence of DC balance in their average voltage levels.

2. (Currently amended) The invention of claim 1, wherein:

said pair of devices comprise a transmitting circuit and a receiving circuit communicating serially with one another on said bus with said plurality of bits, said bits being digital bits having voltage level values of HIGH and LOW; and

said transmitting circuit and said receiving circuit being in substantially close proximity to one another, wherein said ~~framed packet~~ frame of bits [are] is characterized by the absence of DC balance in the average voltage levels of said bits.

3. (Original) The invention of claim 2, wherein:

said transmitting and said receiving circuits share the same ground, said circuits transmitting and receiving a plurality of said frames on said bus.

4. (Original) The invention of claim 3, wherein:

said framing cycle comprises a predetermined number of bits for control by said devices, with a first predetermined number of said predetermined framing cycle bits designated for carrying first control information, and a second, leftover predetermined number of said framing cycle bits designated for carrying second control information.

5. (Previously presented) The invention of claim 3, wherein:

said first predetermined number of said framing cycle bits carry bits that alternate in value between HIGH and LOW between successive frames of said plurality of frames between transmitting and receiving circuits.

6. (Original) The invention of claim 5, wherein:

said leftover control bits are used to carry second control information used by said devices for control of the communication between said devices.

7. (Original) The invention of claim 6, wherein:

said leftover control bits are selected from the group consisting of bits for error correction, bits for CRC error correction, bits for the control of back channel, bits for pointing to reference one of said data cycles transmitted between said plurality of transmitting and receiving circuits, and bits that have a NULL value.

8. (Original) The invention of claim 6, wherein:

said leftover control bits are used by said devices for referencing a data cycle.

9. (Original) The invention of claim 6, wherein:

a plurality of leftover control bits of number N from a consecutive plurality of said frames are combined by said circuits to reference a plurality of data cycles, with the maximum number Y of data cycles that can be referenced by said leftover bits determined by the formula $Y = 2N$.

10. (Original) The invention of claim 4, wherein:

said leftover control bits are used by said circuits for error correction of said frames.

11. (Original) The invention of claim 10, wherein:

said leftover control bits used for error correction by said circuits are for polynomial code checksum error detection; and,

said transmitting and receiving circuits are in synchronous communication.

12. (Previously presented) The invention of claim 4, further comprising:

a plurality of said transmitting and receiving circuits, a plurality of said serial buses, each of said plurality of circuits sharing a serial bus, with one transmitting circuit and one receiving circuit on each of said plurality of serial buses, to form a parallel configuration;

wherein said transmitting and receiving circuits are in synchronous communication, and

wherein said plurality of circuits send and receive a plurality of said frames along said serial buses arranged in parallel.

13. (Original) The invention of claim 12, wherein:

said second predetermined number of leftover control bits are used to reference one of said data cycles.

14. (Original) The invention of claim 13, wherein:

a plurality of said second predetermined number of leftover control bits from a consecutive plurality of frames are used to reference a plurality of data cycles transmitted between said plurality of transmitting and receiving circuits, with the maximum number Y of data cycles that can be referenced by a number N of said leftover bits determined by the formula $Y = 2^N$.

15. (Original) The invention of claim 14, wherein:

said frame comprises one framing cycle for every nineteen data cycles, and said framing cycle comprises an octet.

16. (Previously presented) The invention of claim 4, wherein:

said first Predetermined number of said framing cycle bits carrying first control information comprising a pair of bitwise values ' 10' that alternate on consecutive frames on said serial bus with the bitwise values '01 '; and,

wherein said framing cycle comprises an octet of bits.

17. (Previously presented) The invention of claim 3, wherein:

said transmitting and receiving circuits are circuits selected from the group consisting of multiplexers, encoders, analog-to-digital converters, serdes, Batcher, banyan and knockout switches, routers (on a card), modems, and data flow machines with the bitwise values '01'; and,

wherein said framing cycle comprises an octet of bits.

18. (Original) The invention of claim 4, wherein:

said first predetermined number of said framing cycle bits carrying first control information comprising a pair of bitwise values '10' that alternate on consecutive frames on said serial bus with the bitwise values '01 '; and,

wherein said framing cycle comprises an octet of bits.

19. (Original) The invention of claim 2, further comprising:

a plurality of said transmitting and receiving circuits, a plurality of said serial buses, each of said plurality of circuits sharing a serial bus, with one transmitting circuit and one receiving circuit on each of said plurality of serial buses, to form a parallel configuration, wherein said transmitting and receiving circuits are in synchronous communication.

20. (Original) The invention of claim 19, wherein:

said transmitting and receiving circuits are circuits selected from the group consisting of multiplexers, encoders, analog-to-digital converters, serdes, Batcher, banyan and knockout switches, routers (on a card), modems, and data flow machines.

21. (Original) The invention of claim 19, wherein:

said transmitting and said receiving circuits share the same ground, said circuits transmitting and receiving a plurality of said frames on said bus; and,

said framing cycle comprises a predetermined number of bits for control, with a first predetermined number of said predetermined framing cycle bits designated for carrying first

control information for said frame, and a second, leftover predetermined number of said framing cycle bits designated for carrying second control information for said frame.

22. (Original) The invention of claim 21, wherein:

said leftover framing cycle bits carry second control information selected from the group consisting of bits for error correction, bits for CRC error correction, bits for the control of back channel, bits for pointing to reference one of said data cycles transmitted between said plurality of transmitting and receiving circuits, and bits that have a NULL value.

23. (Original) The invention of claim 22, wherein:

said frame comprises one framing cycle for every nineteen data cycles, and said framing cycle comprises an octet of bits.

24. (Currently amended) An improved protocol for digital transmission of data in frames comprising:

a plurality of digital bits in a predetermined format defining a frame, said predetermined format comprising a plurality of digital bits comprising bits forming a frame cycle and bits forming a data cycle;

said frame cycle carrying information relating to the protocol for said frame, and said data cycle carrying informational data to be transmitted by said protocol;

a plurality of said frames, wherein said protocol is characterized by the voltage levels of bits on successive frame cycles and said successive data cycles on consecutive frames having no DC balance, and wherein said successive framing cycles provide a minimum bit transition frequency allowing clock recovery by a device receiving said frames.

25. (Original) The invention of claim 24, wherein:

said frame cycle bits comprise bits delimiting said frame and leftover bits, said leftover bits used for the carrying control information for said frame.

26. (Original) The invention of claim 25, wherein said leftover bits are used for error correction.

27. (Original) The invention of claim 25, wherein said leftover bits are used for pointing to data cycles.

28. (Original) The invention of claim 25, wherein said bits delimiting said frame alternate between bitwise values of '10' and '01' on successive frames.

29. (Original) The invention of claim 25, wherein said leftover bits from consecutive frames are combined to reference a plurality of data cycles, with the maximum number Y of data cycles that can be referenced by a number N of said leftover bits determined by the formula $Y = 2^N$.

30. (Original) The invention of claim 29, wherein said protocol is used for synchronous communication.

31. (Original) The invention of claim 30, further comprising:

a plurality of transmitting and receiving circuits, a plurality of serial buses, each of said plurality of circuits sharing between a pair of transmitting and receiving circuits one of said plurality of serial buses, to form a parallel configuration;

said transmitting and receiving circuits in synchronous communication;

wherein said protocol is used between a plurality of circuits in serial communication with one another, said plurality of circuits arranged in parallel.

32. (Currently amended) A method of transmitting data according to a protocol comprising the steps of:

forming a packet of data comprising digital bits having a HIGH voltage and a LOW voltage;

parsing said packet of data into a plurality of frames;

parsing each of said frames into a plurality of bits that form a data cycle and a plurality of bits that form a frame cycle;

transmitting said plurality of frames;

wherein said plurality of frames, said data cycles and said frame cycles are comprised of bits characterized by having an absence of DC balance in their HIGH and LOW voltages, and wherein the framing cycles provide a minimum bit transition frequency allowing clock recovery by a receiving device.

33. (Original) The method of transmitting data according to claim 32, further comprising the step of:

connecting at least two devices with a bus that transmits data serially between said devices, said devices utilizing said protocol on said bus to communicate with one another.

34. (Original) The invention of claim 33, further comprising the steps of:

fabricating said devices from electronic circuits, said electronic circuits in substantial close proximity to one another and sharing a common ground.

35. (Original) The method of transmitting data according to claim 33, further comprising the step of:

forming a parallel configuration from a plurality of said serially communicating devices, with each said serial bus providing communication between said two electrical devices, and said plurality of serially communicating devices arranged in parallel to one another.

36. (Original) The method of transmitting data according to claim 32, further comprising the steps of:

parsing said frame cycle into a predetermined number of bits for control, with a first predetermined number of said predetermined framing cycle bits designated for carrying first control information, and a second, leftover predetermined number of said framing cycle bits designated for carrying second control information.

37. (Original) The invention of claim 36, further comprising the steps of:

utilizing said first predetermined number of said frame cycle bits to carry bits that alternate in value between HIGH and LOW between successive frames of said plurality of frames between transmitting and receiving circuits;

utilizing said leftover control bits are for referencing a data cycle within one of said plurality of frames in said parallel configuration, with the maximum number Y of data cycles that can be referenced by a number N of said leftover bits determined by the formula $Y = 2^N$.

38. (Cancelled).

39. (Previously presented) An improved protocol for devices comprising:

a plurality of serial buses;

a plurality of said transmitting and receiving circuits, with one transmitting circuit and one receiving circuit sharing each of said plurality of serial buses, to form a parallel configuration, wherein each pair of said circuits share a same ground and are in substantially close proximity to one another;

synchronous, serial communication on said serial bus between said circuits utilizing a protocol comprising a plurality of digital bits in a predetermined format comprising a frame, said bits being digital bits having voltage level values of HIGH and LOW;

wherein said plurality of circuits send and receive a plurality of said frames along said serial buses arranged in parallel, wherein each of said frames comprise a plurality of digital bits forming a framing cycle and a plurality of bits forming a data cycle, said framing cycle comprising a predetermined number of bits for control by said devices, with a first predetermined number of said predetermined framing cycle bits designated for carrying first control information, and a second, leftover predetermined number of said framing cycle bits designated for carrying second control information.

said devices formatting said digital bits in said predetermined frame format; said devices having no requirement for DC balance when formatting said digital bits, wherein said bits of said frame have an absence of DC balance in the average voltage levels of said bits.

40. (Previously presented) An improved protocol for devices comprising:

a plurality of serial buses;

a plurality of said transmitting and receiving circuits selected from the group consisting of multiplexers, encoders, analog-to-digital converters, serdes, Batcher, banyan and knockout

switches, routers (on a card), modems, and data flow machines, with one transmitting circuit and one receiving circuit sharing each of said plurality of serial buses, to form a parallel configuration, wherein each pair of said circuits share a same ground and are in substantially close proximity to one another;

synchronous, serial communication on said serial bus between said circuits utilizing a protocol comprising a plurality of digital bits in a predetermined format comprising a frame, said bits being digital bits having voltage level values of HIGH and LOW;

wherein said plurality of circuits send and receive a plurality of said frames along said serial buses arranged in parallel, wherein each of said frames comprise a plurality of digital bits forming a framing cycle and a plurality of bits forming a data cycle, wherein said frame comprises one framing cycle for every nineteen data cycles, and said framing cycle comprises an octet of bits,

said framing cycle comprising a predetermined number of bits for control by said devices, with a first predetermined number of said predetermined framing cycle bits designated for carrying first control information, and a second, leftover predetermined number of said framing cycle bits designated for carrying second control information, said leftover framing cycle bits carry second control information selected from the group consisting of bits for error correction, bits for CRC error correction, bits for the control of back channel, bits for pointing to reference one of said data cycles transmitted between said plurality of transmitting and receiving circuits, and bits that have a NULL value;

said devices formatting said digital bits in said predetermined frame format; said devices having no requirement for DC balance when formatting said digital bits, wherein said bits of said frame have an absence of DC balance in the average voltage levels of said bits.

41. (Previously presented) An improved protocol for digital transmission of data in frames comprising:

a plurality of digital bits in a predetermined format defining a frame, said predetermined format comprising a plurality of digital bits comprising bits forming a frame cycle and bits forming a data cycle, wherein said frame cycle bits comprise bits delimiting said frame and leftover bits, said leftover bits used for error correction and for pointing to data cycle;

said frame cycle carrying information relating to the protocol for said frame, and said data cycle carrying informational data to be transmitted by said protocol;

a plurality of said frames, wherein said protocol is characterized by the voltage levels of bits on successive frame cycles and said successive data cycles on consecutive frames having no DC balance.

42. (Previously presented) An improved protocol for digital transmission of data in frames comprising:

a plurality of digital bits in a predetermined format defining a frame, said predetermined format comprising a plurality of digital bits comprising bits forming a frame cycle and bits forming a data cycle, wherein said frame cycle bits comprise bits delimiting said frame and leftover bits, said leftover bits used for carrying control information for said frame, wherein said bits delimiting said frame alternate between bitwise values of '10' and '01' on successive frames;

said frame cycle carrying information relating to the protocol for said frame, and said data cycle carrying informational data to be transmitted by said protocol;

a plurality of said frames, wherein said protocol is characterized by the voltage levels of bits on successive frame cycles and said successive data cycles on consecutive frames having no DC balance.

43. (Previously presented) An improved protocol for digital transmission of data in frames comprising:

a plurality of digital bits in a predetermined format defining a frame, said predetermined format comprising a plurality of digital bits comprising bits forming a frame cycle and bits forming a data cycle, wherein said frame cycle bits comprise bits delimiting said frame and leftover bits, said leftover bits used for carrying control information for said frame, wherein said leftover bits from consecutive frames are combined to reference a plurality of data cycles, with a maximum number Y of data cycles that can be referenced by a number N of said leftover bits determined by the formula $Y = 2^N$;

said frame cycle carrying information relating to the protocol for said frame, and said data cycle carrying informational data to be transmitted by said protocol;

a plurality of said frames, wherein said protocol is characterized by the voltage levels of bits on successive frame cycles and said successive data cycles on consecutive frames having no DC balance.

44. (Previously presented) A method of transmitting data according to a protocol comprising the steps of:

forming a parallel configuration from a plurality of serial busses and a plurality of said serially communicating devices, with each said serial bus providing communication between two of said serially communicating devices, and said plurality of serially communicating devices arranged in parallel to one another, said devices utilizing said protocol on said bus to communicate with one another by;

forming a packet of data comprising digital bits having a HIGH voltage and a LOW

voltage;

parsing said packet of data into a plurality of frames;

parsing each of said frames into a plurality of bits that form a data cycle and a plurality of bits that form a frame cycle;

transmitting said plurality of frames;

wherein said plurality of frames, said data cycles and said frame cycles are comprised of bits characterized by having an absence of DC balance in their HIGH and LOW voltages.

45. (Cancelled).

46. (Currently amended) A system for providing improved protocol for devices comprising:

a backplane;

a plurality of serial buses framed within the backplane; and

a plurality of ~~said~~ transmitting and receiving circuits coupled to said plurality of serial buses such that one transmitting circuit and one receiving circuit share a respective one of said plurality of serial buses, thereby forming a parallel configuration, wherein each pair of said circuits share a same ground;

said circuits synchronously communicating a plurality of digital bits across said serial buses utilizing a protocol that formats said digital bits into frames, wherein each of said frames includes one framing cycle and a plurality of data cycles, wherein the framing cycle provides a minimum bit transition frequency allowing the receiving ~~thereby reducing bus overhead and enabling said~~ circuits to perform clock recovery;

said circuits having no requirement for DC balance when formatting said digital bits, such

that voltage levels of said bits of said frames have an absence of DC balance.

47. (New) An improved protocol for devices comprising:

a plurality of serial buses for communication between a pair of devices, wherein said pair of devices comprise a plurality of transmitting and receiving circuits communicating serially with one another on said serial buses with said plurality of bits, said bits being digital bits having voltage level values of HIGH and LOW, wherein each of said plurality of circuits sharing a serial bus, with one transmitting circuit and one receiving circuit on each of said plurality of serial buses, to form a parallel configuration, wherein said transmitting and receiving circuits are in synchronous communication, said transmitting circuit and said receiving circuit being in substantially close proximity to one another,

communication on said serial bus between said devices utilizing a protocol comprising a plurality of digital bits in a predetermined format, said predetermined format comprising a frame;

said frame comprising a plurality of digital bits forming a framing cycle and a plurality of bits forming a data cycle;

said devices formatting said digital bits in said predetermined frame format; said devices having no requirement for DC balance when formatting said digital bits, wherein said bits of said frame have an absence of DC balance in their average voltage levels.

48. (New) An improved protocol for digital transmission of data in frames comprising:

a plurality of digital bits in a predetermined format defining a frame, said predetermined format comprising a plurality of digital bits comprising bits forming a frame cycle and bits forming a data cycle, wherein said frame cycle bits comprise bits delimiting said frame and leftover bits, said leftover bits used for carrying control information for said frame and for

pointing to data cycles;

said frame cycle carrying information relating to the protocol for said frame, and said data cycle carrying informational data to be transmitted by said protocol; and

a plurality of said frames, wherein said protocol is characterized by the voltage levels of bits on successive frame cycles and said successive data cycles on consecutive frames having no DC balance.